

The diagram illustrates a 5-stage pipeline with 5 registers. Each stage contains a multiplexer, a 4-bit adder, and a 4-bit register. The diagram shows the flow of data and control signals between these components across five stages.

Stage 1: The multiplexer selects between the input and the output of the adder. The adder takes the input and a constant '1' as inputs. The output of the adder is stored in the register.

Stage 2: The multiplexer selects between the input and the output of the adder. The adder takes the input and the output of the register from Stage 1 as inputs. The output of the adder is stored in the register.

Stage 3: The multiplexer selects between the input and the output of the adder. The adder takes the input and the output of the register from Stage 2 as inputs. The output of the adder is stored in the register.

Stage 4: The multiplexer selects between the input and the output of the adder. The adder takes the input and the output of the register from Stage 3 as inputs. The output of the adder is stored in the register.

Stage 5: The multiplexer selects between the input and the output of the adder. The adder takes the input and the output of the register from Stage 4 as inputs. The output of the adder is stored in the register.

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